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| Abbreviation | Datasheet | Description | Time |
| T\_ast | Address setup time | Time between D/C line change and WR or RD fall | 4.83us |
| T\_aht | Address hold time | Time between WR or RD rise and D/C change | 10us |
| T\_chw | Chip select H pulse width | Time CS is high between transfers |  |
| T\_cs | Chip select setup time | Time that CS is low before WR or RD comes high | 120us |
| T\_rcs | Chip select setup time (read ID) |  |  |
| T\_rcs | Chip select setup time (read FM) |  |  |
| T\_csf | Chip select wait time | Time from CS rise to WR fall? | NA |
| T\_csh | Chip select hold time | Time from WR rise to CS rise. | 10us |
| T\_wc | Write cycle | Time from WR fall to WR fall | 19us |
| T\_wrh | Control pulse high duration | Time that WR is high | 7us |
| T\_wrl | Control pulse low duration | Time that WR is low | 12us |
| T\_rc (ID) | Read cycle (ID) |  |  |
| T\_rdh (ID) | Control pulse high duration (ID) |  |  |
| T\_rdl (ID) | Control pulse low duration (ID) |  |  |
| T\_dst | Data setup time | Time that data is on the bus before WR goes high | 2.5us |
| T\_dht | Data hold time | Time from WR going high to data changing. | 14us |
| T\_odh | Output disable time. | Unknown |  |

Diagram

Description automatically generated